**Remarks/Arguments**

Applicants thank Examiner Lewis for her careful examination of this application and clear explanation of the claim rejections. In response, applicants cancel claims 1-24 and insert new claims 25-27.

New claim 25 describes a device that has the following limitations:

a. an integrated circuit chip having a plurality of contact pads dimensioned smaller than 50 $\mu$m across and spaced apart less than 100 $\mu$m center to center;

b. a thin-film interposer having a single-layered insulating film;

c. substantially flat, electrically conductive lines disposed on only one side of the insulating film; electrically conductive paths extending through the interposer, contacting the conductive lines and forming exit ports on a second side of the insulating film; and

d. thermo-compressed electrical coupling members disposed between the contact pads and conductive lines, connecting the chip to the interposer.

Claim 25 is fully supported in the original specification and original drawing figures: The contact-pad size and pitch limitation in (a) can be found, for example, in page 2 of the original specification, lines 16-22; the single-layered insulating film limitation in (b) can be found, for example, in original drawing Fig. 1 ; the substantially-flat-electrically-conductive-line limitation in (c) can be found, for example, in page 10 of the original specification, line 31 bridging page 11, line10; and the thermo-compressed-electrical-coupling-member limitation in (d) can be found, for example, in page 16 of the original specification, lines 30-32.

The cited references do not disclose all the limitations in claim 25:

1. Rahim discloses a circuit structure in which IC contact pads 46 and 48 are connected to corresponding grid-array substrate pads 24 and 34 using solder balls 50.[1] Because it uses solder balls, it is constrained to the solder-ball limited of 160 $\mu$m and

[1] US 6,362,525, col. 7, ll. 23-25.

will not be able to design a contact pads dimensioned smaller than 50 μm across and spaced apart less than 100 μm center to center.[2] Rahim also discloses a circuit board that has insulating layers 22 interposed between conductive layers 12 and 16 and between layers 16 and 18.[3] Therefore, it does not disclose a thin-film interposer having a single-layered insulating film and electrically conductive lines disposed on only one side of the insulating film. Furthermore, because Rahim uses solder balls to connect the chip to the circuit balls, it does not disclose a thermo-compressed electrical coupling members disposed between the contact pads and conductive lines, connecting the chip to the interposer.

2. Hino discloses a semiconductor device that uses a film carrier that is a flexible insulator layer 6 in which a conductive circuit 5 is embedded so that it will not be exposed at the both surfaces 6a and 6b of the insulator layer 6.[4] This film carrier does not anticipate a thin-film interposer that has a single-layered insulating film with substantially flat, electrically conductive lines disposed on only one side of it. Hino also fails to disclose thermo-compressed electrical coupling members disposed between the contact pads and conductive lines, connecting the chip to the interposer. In addition, Hino's bumps 9 and 10 on both sides of the film carrier clearly do not anticipate substantially flat, electrically conductive lines disposed on only one side of the insulating film.

3. Lee discloses an interposer inserted between a chip 10 and a substrate 14 where the chip 10 has a ball grid array of solder balls 12 disposed on the surface of chip 10.[5] Again, the solder-ball will limit the chip design, prevents it to have contact pads dimensioned smaller than 50 μm across and spaced apart less than 100 μm center to center. In addition, as clearly depicted in Figs. 1-4, there are top contact layer 30 and bottom layer 26 on the surfaces of interposer 18, contrary to the limitation of an insulating film with substantially flat, electrically conductive lines disposed on only one side. Furthermore, Lee does not disclose thermo-compressed electrical coupling

[2] See, Specification, p. 2, ll. 16-18.
[3] Supra, col. 7, ll. 66-67.
[4] See, US 6,157,084, col.4, ll. 26-28.
[5] US 6,050,832, col. 37-46.

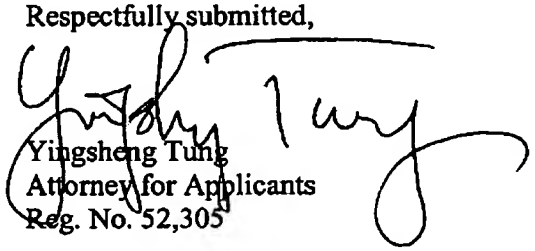
members disposed between the contact pads and conductive lines, connecting the chip to the interposer.

In summary, all limitations of claim 25 are not disclosed in the cited references and there is no suggestion in any of the references to combine all the limitations of claim 25. Therefore, claim is not anticipated by nor rendered obvious over the references. Applicants respectfully submit that claim 25 stands patentable over the references.

Claims 26 and 27 depend directly on patentable claim 25, so they stand patentable by virtue of their dependency.

Applicants respectfully submit that the amended application is in allowable form and claims 25-27 distinguish over the references and stand patentable. Applicants respectfully request further examination of this application and timely allowance of the pending claims.

Respectfully submitted,



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